RESPONSE

The present Response is in response to the Office Action having a mailing date of September 12, 2003. Claims 1-9 are pending in the present Application.

In the above-identified Office Action, the Examiner rejected claims 1-9 under 35 U.S.C. § 103 as being unpatentable over Japanese Patent JP411204854A (Mizushima).

Applicant respectfully disagrees with the Examiner's rejection. Independent claim 1 recites

> [a] magnetic memory cell comprising:
> a magnetic tunneling junction including a first ferromagnetic layer, a second ferromagnetic layer and an insulating layer between the first ferromagnetic layer and the second ferromagnetic layer; and
> a transistor having a source, a drain and a gate, the gate of the transistor being coupled to a first end of the magnetic tunneling junction, the source of the transistor being coupled to a second end the magnetic tunneling junction, the drain of the transistor being coupled with an output for reading the magnetic memory cell.

Similarly, independent claim 5 recites:

> [a] magnetic memory comprising:
> a plurality of memory cells arranged in an array including a plurality of rows and a plurality of columns, each of the plurality of memory cells including a magnetic tunneling junction and a transistor having a source, a drain and a gate, the gate of the transistor being coupled to a first end of the magnetic tunneling junction, the source of the transistor being coupled to a second end of the magnetic tunneling junction, the drain of the transistor being coupled with an output for reading the magnetic memory cell;
> a plurality of row lines coupled to the plurality of rows, the plurality of row lines coupled to gate of the transistor in each of the plurality of memory cells in the plurality of rows;
> a row selector coupled to the plurality of row lines for selecting between the plurality of row lines and providing a current to a selected row of the plurality of rows.

Thus, the magnetic memory cells of claim 1 and claim 5 include a magnetic tunneling junction having a first end coupled to the gate of a transistor and a second end coupled to the source of the transistor. Claims 1 and 5 also recite that the output is coupled to the drain of the transistor.

One embodiment of such a memory cell is depicted in Figure 3 of the present application. As can be seen, one end of the magnetic tunneling junction 104 is connected to the gate of the transistor 102, while the other end of the magnetic tunneling junction 104 is connected to the source of the transistor 102. The drain of the transistor is coupled to the output 108. Because of the configuration of the magnetic tunneling junction 104, the transistor, and the output, the magnitude of the signal, as well as the difference in signal between different states of the magnetic tunneling junction, are significantly larger. Specification, page 7, lines 16-24. As a result, performance is improved.

The cited portions of Mizushima fail to teach or suggest the recited magnetic tunneling junction coupled to the gate and source of the transistor in combination with the drain of the transistor being coupled to the output. In particular, Mizushima does not couple the source of the transistor with a second end of the magnetic tunneling junction and connect the drain of the transistor with the output. As can be determined from the Abstract of Mizushima, item 4 of Mizushima is a "**gate resistor**", item 1 is a magnetic tunnel junction device, and item 2 is a transistor. Therefore, the cited figure of Mizushima, Figure 10, does not include a magnetic tunnel junction device 1. Instead, only the gate resistor 4 and other devices 2, 3, and 9 are depicted. Furthermore, the gate resistor 4 is coupled to the gate of the transistor 2 and ground. The drain of the transistor 2 is coupled to ground, while the source is coupled to the output via resistor 3. Thus, the magnetic tunnel junction is not present in Figure 10. Even if the gate resistor 4 is considered to include a magnetic tunnel junction, to which the Applicant does not agree, the source of the transistor 2 is not coupled to a second end of the gate resistor. Instead, the drain of the transistor 2, could be considered to be connected with the second end of the gate resistor. Furthermore, the source, rather than the drain, of the transistor 2 of Mizushima is coupled with the output.

Consequently, the connections between the gate resistor, the transistor and the output are different in Figure 10 of Mizushima than is recited in claims 1 and 5.

Even if Figure 1 of Mizushima, which includes a magnetic tunneling junction 1, is considered, Mizushima still fails to teach or suggest the configuration of the magnetic tunneling junction, the transistor and the output of claims 1 and 5. The magnetic tunneling junction 1 is coupled with the gate of the transistor 2 of Mizushima. The source of the transistor 2 is also connected to the magnetic tunneling junction 1. However, the source of the transistor 2 is also coupled to the output via the resistor 3. Consequently, in contrast to the magnetic memory cell and magnetic memory recited in claims 1 and 5, the drain of the transistor is not coupled to the output.

Thus, the cited portions of Mizushima fail to describe the recited magnetic tunneling junction coupled to the gate and source of the transistor in combination with the drain of the transistor being coupled to the output. Mizushima, therefore, fails to teach or suggest the magnetic memory cell and magnetic memory recited in claims 1 and 5, respectively.

Claims 2-4 and 6-9 depend upon claims 1 and 5, respectively. Consequently, the arguments herein apply with full force to claims 2-4 and 6-9. Accordingly, Applicant respectfully submits that claims 2-4 and 6-9 are allowable over the cited references.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

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